

In re Patent Application of:  
**BORGATTI ET AL.**  
Serial No. **10/768,401**  
Filing Date: **JANUARY 30, 2004**

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**In the Claims:**

Claims 1-9 (Cancelled).

10. (Previously Presented) A dynamically reconfigurable processing unit comprising:

a microprocessor;

an embedded Flash memory for non-volatile storage of code, data and bit-streams, said embedded Flash memory comprising a field programmable gate array (FPGA) port;

a direct memory access (DMA) channel; and

an S-RAM embedded FPGA for FPGA reconfigurations, said S-RAM embedded FPGA comprising an FPGA programming interface connected to the FPGA port of said embedded Flash memory through said DMA channel;

said microprocessor, said embedded Flash memory, said DMA channel and said S-RAM embedded FPGA being integrated as a single chip.

11. (Previously Presented) A dynamically reconfigurable processing unit according to Claim 10, wherein said embedded Flash memory further comprises a code port and a data port; and wherein said DMA channel handles bit-stream transfers while said microprocessor fetches instructions and data from the code and data ports.

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12. (Previously Presented) A dynamically reconfigurable processing unit according to Claim 10, wherein said embedded Flash memory comprises:

- a modular array structure comprising N memory modules;
- a power memory arbiter (PMA); and
- a charge pump connected to said PMA and being shared among said N memory modules.

13. (Previously Presented) A dynamically reconfigurable processing unit according to Claim 10, further comprising a system bus, and coprocessors connected to said system bus; wherein said S-RAM embedded FPGA comprises:

- an instruction extension interface for extending a datapath of said microprocessor for supporting a set of additional microprocessor instructions;
- a master/slave interface for supporting said coprocessors; and
- an input/output interface for interfacing with external units or sensors with application-specific communication protocols.

14. (Previously Presented) A dynamically reconfigurable processing unit according to Claim 11, wherein the code port of said embedded Flash memory is for optimizing random access time and an application system supported by the reconfigurable processing unit; the data port of said embedded Flash memory is for allowing access to application data for

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modification thereof; and the FPGA port of said embedded Flash memory is for providing serial access for downloading the bit-streams for an embedded FPGA configuration.

15. (Previously Presented) A dynamically reconfigurable processing unit according to Claim 11, wherein the FPGA port of said embedded Flash memory comprises four configuration registers replicating information stored in the code port to be used for writing data for embedded FPGA configurations.

16. (Previously Presented) A dynamically reconfigurable processing unit according to Claim 14, wherein the FPGA port uses a chip select signal to access addressable memory space, and a burst enable signal to allow burst serial access.

17. (Previously Presented) A dynamically reconfigurable processing unit according to Claim 10, further comprising a system bus connected to said DMA channel and said embedded Flash memory.

18. (Previously Presented) A dynamically reconfigurable processing unit according to Claim 14, wherein said embedded Flash memory comprises four modules, each module being arranged in at least three programmable user-defined partitions, with each partition being dedicated to a corresponding port.

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19. (Previously Presented) A reconfigurable processing unit comprising:

a microprocessor;

a system bus connected to said microprocessor;

an embedded Flash memory comprising a code port and a data port connected to said system bus for interfacing with said microprocessor, and a field programmable gate array (FPGA) port;

a direct memory access (DMA) channel connected to said system bus and to the FPGA port of said embedded Flash memory; and

an embedded FPGA for FPGA reconfigurations and comprising an FPGA programming interface connected to said DMA channel for interfacing with the FPGA port of said Flash memory.

20. (Previously Presented) A reconfigurable processing unit according to Claim 19, wherein said microprocessor, said embedded Flash memory, said DMA channel and said embedded FPGA are integrated as a single chip.

21. (Previously Presented) A reconfigurable processing unit according to Claim 19, wherein said embedded FPGA comprises an S-RAM embedded FPGA.

22. (Previously Presented) A reconfigurable processing unit according to Claim 19, wherein said embedded Flash memory comprises:

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a modular array structure comprising N memory modules;  
a power memory arbiter (PMA); and  
a charge pump connected to said PMA and being shared  
among said N memory modules.

23. (Previously Presented) A reconfigurable processing unit according to Claim 19, further comprising coprocessors connected to said system bus; wherein said embedded FPGA comprises:

an instruction extension interface for extending a datapath of said microprocessor for supporting a set of additional microprocessor instructions;

a master/slave interface for supporting said coprocessors; and

an input/output interface for interfacing with external units or sensors with application-specific communication protocols.

24. (Previously Presented) A reconfigurable processing unit according to Claim 19, wherein the code port of said embedded Flash memory is for optimizing random access time and an application system supported by the reconfigurable processing unit; the data port of said embedded Flash memory is for allowing access to application data for modification thereof; and the FPGA port of said embedded Flash memory is for providing serial access for downloading bit-streams for an embedded FPGA configuration.

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25. (Previously Presented) A reconfigurable processing unit according to Claim 19, wherein the FPGA port of said embedded Flash memory comprises four configuration registers replicating information stored in the code port to be used for writing data for embedded FPGA configurations.

26. (Previously Presented) A reconfigurable processing unit according to Claim 24, wherein the FPGA port uses a chip select signal to access addressable memory space, and a burst enable signal to allow burst serial access.

27. (Previously Presented) A reconfigurable processing unit according to Claim 19, wherein said embedded Flash memory comprises four modules, each module being arranged in at least three programmable user-defined partitions, with each partition being dedicated to a corresponding port.

28. (Previously Presented) A method for making a reconfigurable processing unit comprising:

connecting a microprocessor to a system bus;

connecting a code port and a data port of an embedded Flash memory to the system bus for interfacing with the microprocessor, the embedded Flash memory also comprising a field programmable gate array (FPGA) port;

connecting a direct memory access (DMA) channel to the system bus and to the FPGA port of the embedded Flash memory; and

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connecting an FPGA programming interface of an embedded FPGA for FPGA reconfigurations to the DMA channel for interfacing with the FPGA port of the embedded Flash memory.

29. (Previously Presented) A method according to Claim 28, wherein the microprocessor, the embedded Flash memory, the DMA channel and the embedded FPGA are integrated as a single chip.

30. (Previously Presented) A method according to Claim 28, wherein the embedded FPGA comprises an S-RAM embedded FPGA.

31. (Previously Presented) A method according to Claim 28, wherein the embedded Flash memory comprises a modular array structure comprising N memory modules, a power memory arbiter (PMA), and a charge pump connected to the PMA and being shared among the N memory modules.

32. (Previously Presented) A method according to Claim 28, further comprising connecting coprocessors to the system bus; wherein the embedded FPGA comprises:

an instruction extension interface for extending a datapath of said microprocessor for supporting a set of additional microprocessor instructions;

a master/slave interface for supporting the coprocessors; and

an input/output interface for interfacing with external

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units or sensors with application-specific communication protocols.

33. (Previously Presented) A method according to Claim 28, wherein the code port of the embedded Flash memory is for optimizing random access time and an application system supported by the reconfigurable processing unit; the data port of the embedded Flash memory is for allowing access to application data for modification thereof; and the FPGA port of the embedded Flash memory is for providing serial access for downloading bit-streams for an embedded FPGA configuration.

34. (Previously Presented) A method according to Claim 28, wherein the FPGA port of the embedded Flash memory comprises four configuration registers replicating information stored in the code port to be used for writing data for embedded FPGA configurations.

35. (Previously Presented) A method according to Claim 33, wherein the FPGA port uses a chip select signal to access addressable memory space, and a burst enable signal to allow burst serial access.

36. (Previously Presented) A method according to Claim 28, wherein the embedded Flash memory comprises four modules, each module being arranged in at least three programmable user-

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defined partitions, with each partition being dedicated to a corresponding port.